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INFORMATION DISCLOSURE STATEMENT BY APPLICANT				Application Number: 10/755,042 Filing Date: January 9, 2004 First Named Inventor: MOU-SHIUNG LIN Art Unit: 2815 Examiner Name: JEROME JACKSON, JR.	
(Use as many sheets as necessary)					
Sheet	1	of	3	Attorney Docket No: 085027-0104	

US PATENT DOCUMENTS

Examiner Initial *	Cite No	Document Number	Publication Date	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
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FOREIGN PATENT DOCUMENTS

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OTHER DOCUMENTS -- NON PATENT LITERATURE DOCUMENTS

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	1	MISTRY, K. et al. "A 45nm Logic Technology with High-k+ Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," IEEE International Electron Devices Meeting (2007) pgs. 247-250	
	2	EDELSTEIN, D.C., "Advantages of Copper Interconnects," Proceedings of the 12th International IEEE VLSI Multilevel Interconnection Conference (1995) pgs. 301-307	
	3	THENG, C. et al. "An Automated Tool Deployment for ESD (Electro-Static-Discharge) Correct-by-Construction Strategy in 90 nm Process," IEEE International Conference on Semiconductor Electronics (2004) pgs. 61-67	
	4	GAO, X. et al. "An improved electrostatic discharge protection structure for reducing triggering voltage and parasitic capacitance," Solid-State Electronics, 27 (2003), pgs. 1105-1110	
	5	YEOH, A. et al. "Copper Die Bumps (First Level Interconnect) and Low-K Dielectrics in 65nm High Volume Manufacturing," Electronic Components and Technology Conference (2006) pgs. 1611-1615	
	6	HU, C-K. et al. "Copper-Polyimide Wiring Technology for VLSI Circuits," Materials Research Society Symposium Proceedings VLSI V (1990) pgs. 369-373	
	7	ROESCH, W. et al. "Cycling copper flip chip interconnects," Microelectronics Reliability, 44 (2004) pgs. 1047-1054	
	8	LEE, Y-H. et al. "Effect of ESD Layout on the Assembly Yield and Reliability," International Electron Devices Meeting (2006) pgs. 1-4	

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	9	YEOH, T-S. "ESD Effects On Power Supply Clamps," Proceedings of the 6th International Symposium on Physical & Failure Analysis of Integrated Circuits (1997) pgs. 121-124	
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	12	JENEI, S. et al. "High Q Inductor Add-on Module in Thick Cu/SiLK™ single damascene," Proceedings from the IEEE International Interconnect Technology Conference (2001) pgs. 107-109	
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	20	MALONEY, T. et al. "Novel Clamp Circuits for IC Power Supply Protection," IEEE Transactions on Components, Packaging, and Manufacturing Technology, Part C, Vol. 19, No. 3 (07-1996) pgs. 150-161	

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	21	GEFFKEN, R. M. "An Overview of Polyimide Use in Integrated Circuits and Packaging," Proceedings of the Third International Symposium on Ultra Large Scale Integration Science and Technology (1991) pgs. 667-677	
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	24	MALONEY, T. et al. "Stacked PMOS Clamps for High Voltage Power Supply Protection," Electrical Overstress/Electrostatic Discharge Symposium Proceedings (1999) pgs. 70-77	
	25	LIN, M.S. et al. "A New System-on-a-Chip (SOC) Technology – High Q Post Passivation Inductors," Proceedings from the 53rd Electronic Components and Technology Conference (05-30-2003) pgs. 1503-1509	
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